two-dimensional code conversion unit 42 is rendered on the liquid crystal mask 40 by the liquid crystal driver 43.

Then, by using this liquid crystal mask 40, exposure is performed at a specific position on each chip with a projection exposure apparatus (not shown) to develop a two-dimensional code pattern inherent to each chip. After this, by implementing the photolithography step and the etching step as in normal processing, a two-dimensional code pattern inherent to each chip is formed. It is to be noted that while an example in which different two-dimensional code patterns are provided for the individual chips is presented above, it foes without saying that a singles two-dimensional code pattern can be formed for all the chips.

As has been explained, in this embodiment, it is possible to add chip ID information for distinguishing the individual chips in a wafer from one another while taking up an extremely small area on the individual chips of the wafer, and thus, individual chips on a wafer surface can be distinguished from one another, which is not possible in the prior art. In addition, by forming two-dimensional code patterns on chips during the wiring step in the wafer process, chip ID information can be recorded for each chip without having to allocate special space for accommodating the two-dimensional code pattern. Furthermore, by utilizing the liquid crystal mask 40 shown in FIG. 4, chip ID information that is different for each chip can be recorded using one mask.

IN THE CLAIMS:

Please amend claim 1, 4, 6, 7, 9, 10 14, 16, 17,18 and 21 as follows:

1. (Four Times Amended) A semiconductor device having at least one semiconductor chip manufactured from a wafer, said semiconductor chip comprising said device

and having a two-dimensional matrix code pattern for information management provided on a surface of said at least one semiconductor chip with the pattern representing chip ID information, and said two-dimensional matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

4. (Thrice Amended) A semiconductor device manufactured using a lead frame, with the lead frame having a two-dimensional matrix code pattern for information management provided on said lead frame to which semiconductor ships are bonded, with the pattern representing frame ID information, and said two-dimensional matrix code pattern is comprised of a plurality of square blocks arranged in a predetermined two-dimensional region.

6. (Amended) A semiconductor device according to claim 4 wherein said frame ID information is made to correspond to chip ID information provided as a two-dimensional matrix code pattern for information management for each chip.

7. (Thrice Amended) A semiconductor device having at least one semiconductor ship sealed by resin, and having a two-dimensional matrix code pattern for information management provided at an outer surface of said resin and representing product ID information, and said two-dimensional matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

9. (Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional matrix code pattern for information management for each chip.

10. (Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional matrix code pattern for information management on a lead frame to which semiconductor chips are bonded.

11. (Thrice Amended) An information management system for semiconductor devices, having at least one semiconductor chip that implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads ship ID information, said chip ID information is provided on said semiconductor chip as a two-dimensional matrix code pattern for information management for each chip, said two-dimensional matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said chip ID information thus read and manages individual semiconductor manufacturing processes based upon said chip ID information thus registered.

14. (Thrice Amended) An information management system for semiconductor device manufactured using a lead frame, which system implements management of information

related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads frame ID information, said frame ID information is provided on said lead frame as a two-dimensional matrix pattern for information management, said two-dimensional matrix code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said frame ID information thus read and manages individual semiconductor manufacturing processes based upon said frame ID information thus registered.

16. (Thrice Amended) An information management system for semiconductor devices having semiconductor chips sealed by resin, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads product ID information, said product ID information is provided as a two-dimensional matrix pattern for information management at an outer surface of said resin, said two-dimensional matrix pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said product ID information thus read and manages a product shipping process based upon said product ID information thus registered.